APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

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Replacement for the paragraph beginning at page 1, line 8:

FIG. 3 is a block diagram showing an example of a conventional video data transfer system. As shown in the figure, video data decoded by a video decoder 11 is sent via a video port 12 to a graphic accelerator 30 having a video input function. Upon receiving video data, the graphic accelerator 30, which comprises a video processor 21, display control circuit 22, and a FIFO memory 24, causes the video processor 21 to perform predetermined signal processing for the received video data and outputs the processed video data to a frame buffer 14 via a frame buffer data bus 13 for storage in an internal off-screen memory 15.

Replacement for the paragraph beginning at page 2, line 22:

The present invention seeks to solve the problems associated with the prior art described above. It is an object of the present invention to provide a video data transfer system which increases the capturing rate of video data to be sent to the system memory.

Replacement for the paragraph beginning at page 4, line 5:

An embodiment of the present invention is described with reference to the attached drawings. FIG. 1 is a block diagram of the embodiment of the video data transfer system according to the present invention. As shown in FIG. 1, a video decoder 11 is connected via a video port 12 to a graphic accelerator 20 which has a video input function. This graphic accelerator 20 is connected to a frame buffer 14 via a frame buffer data bus 13, to a system memory 18 via a system bus 17, and to a display 16. The graphic accelerator 20 has a video processor 21, a display control circuit 22, a gate 23, and a FIFO memory 24.

Replacement for the paragraph beginning at page 6, line 24:

The configuration of the embodiment according to the present invention is detailed with reference to FIG. 1. The graphic accelerator 20 with a video input function is implemented as a large scale integrated circuit (LSI). It comprises the video processor 21 which reduces the size of video data according to the YUV 16 bits, the real time output path 25 which is a 64-bit internal bus through which video data from the video processor 21 is sent to the display control circuit 22 via the frame buffer 14, and the capturing-only path 26 which is a 32-bit internal bus through which video data from the video processor 21 is sent to the FIFO memory 24 via the gate 23.

CLAIMS (with indication of amended or new):

1. (Amended) A video data transfer system comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a capturing path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus; and

a gate in said capturing path, said gate being controllable to permit said video data to pass when received from said video processor.

2. (Amended) A video data transfer system, comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a capturing path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus, wherein

said real time output path comprises:

an off-screen memory which receives video data from said video processor via a data bus and stores video data therein, said off-screen memory being in the frame buffer; and

a display control circuit which receives video data read from said off-screen memory via said data bus for enlargement and interpolation processing and transfers processed results to said display, and wherein

said capturing path comprises:

a gate which is opened only when video data is received from said video processor for capturing; and

memory means for storing said video data sent through said gate and for transferring said video data to said system bus.

4. (Amended) A video data transfer system as defined in claim 1, further comprising:

a capture path memory in said capturing path;

said capture path memory being connected to said gate; and

said capture path memory being operable to store said video data passed by said gate.

6. (Amended) A video data transfer system as defined in claim 5, wherein said real time output path further comprises:

an off-screen memory effective to receive said video data from said video processor via a data bus and store said video data therein; and wherein

said off-screen memory is in said frame buffer.

7. (Amended) A video data transfer method, comprising:

providing video data from a video processor to a plurality of paths independent of each other;

sending said video data to a display through a frame buffer in at least one of said independent paths operating as a real time output path;

sending said video data to a system memory through a system bus in at least another of said independent paths operating as a capture path; and

controlling said capture path to permit said video data to pass to said system memory when said video data is to be captured.

8. (Amended) A video data transfer method as defined in claim 7, further comprising storing said video data in a capture path memory in said capture path when said video data is permitted to pass to said system memory.

12. (Amended) A video data transfer method as defined in claim 11, further comprising controlling said capture path to prevent said video data from being stored in said capture path memory when said capture path memory contains said at least one of a field and a frame delimiter.

13. (New) A video data transfer system comprising:

a video processor, the video processor is effective to receive video data, determine whether the video data is to be captured, and process the video data to produce processed video data;

a gate coupled to the video processor, the gate being effective to receive the processed video data, the gate further selectively outputs the processed video data when the video processor determines that the video data is to be captured; and

a display control circuit coupled to the video processor.

14. (New) A method of transferring video data, the method comprising:

receiving video data;

determining whether the video data is to be captured;

processing the video data to produce processed data;

forwarding the processed video data to a first path, the first path including a display control circuit; and

forwarding the processed video data to a second path when the determining indicates that the video data is to be captured;

wherein the first and second paths are distinct.